IN THE SPECIFICATION

Please replace the first paragraph on page 2, lines 4-7 with the following amended paragraph:

The present application is related to co-pending application entitled, "Sense Amplifier for a Memory Array", Serial Number: ~~Unassigned,~~ 10/768,098, Filed: ~~on even date herewith, serial number: unassigned,~~ 02/02/2004, attorney docket number: TI-36686, assigned to common assignee, and naming as inventors: Balasuramanian *et al.*

Please add the following new paragraph to page 4, after line 5:

Summary of Invention

A sense amplifier senses a signal received on a bit line to generate a bit, and a latch latches the bit at a time point specified by a latch enable signal. A tracking circuit generates the latch enable signal in an appropriate time window. The tracking circuit contains a dummy sense amplifier implemented similar to the actual sense amplifier and a dummy column from which the actual sense amplifier senses a signal received upon accessing the dummy memory array. The latch enable signal may be generated after the dummy sense amplifier generates a bit representing the sensed signal. The time taken by the dummy

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sense amplifier to generate the bit depends on the load offered by the dummy memory array. Accordingly, the dummy memory array is designed to offer sufficient load to ensure that the latch enable signal is generated in an appropriate time window.

Please replace the first paragraph on page 9, lines 5-10 with the following amended paragraph:

Word lines [[122-1]] 122-3 through 122-N are contained within bus 122 (of Figure 1A), with only one of the word lines being enabled during a read operation. Each word line turns on all the cells in the corresponding enabled row, and signals representing the data stored in all the cells of the corresponding row are provided on corresponding bit lines 113-1 through 113-M. Only one of the bit lines 113-1 through [[113-M]] 113-(M-1) is selected (on line 135) by column decoder 130, and the signal on the selected line is sensed (and thus read) as a 0 or 1.

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